Integrated Circuits in Detector Systems

- The Promise and the Pitfalls

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Outline:

I. Some representative ICs from high-energy physics

II. Some Common Problems

a) Design and Debugging process

b) Lessons Learned

c) What does it take?

d) Sociology

Over the past 15 years high-energy physics detectors have undergone a radical transformation.

Old style: detector + front-end electronics + DAQ were separate entities. Typically one cable per channel.

New style: detectors + front-end electronics + part of DAQ are highly integrated to allow high sensor density, simplify readout

Subsystems with millions of channels now common in new detectors

Possible through application of microelectronics technology to specific needs of HEP.

Unique combination of

low noise
speed
low power
mixed analog/digital
packaging

Full custom design allows optimization of transistor geometries + circuit topologies not practical in conventional designs

Astrophysics is now at the verge of a similar development

a) SNAP (S. Perlmutter, M. Levi, et al.)

Satellite-based supernova search
~ 1 Gpixel arrays of CCDs (LBNL technology)

b) POLARBEAR
(A. Lee, W. Holzapfel, P. Richards, G. Smoot, H. Spieler)

Next-generation CMB experiment (polarization)
~ 3000 superconducting transition-edge sensors at 0.3 K

1000 TES elements have been monolithically fabricated on a wafer (Jan Gildemeister)

major challenges: yield, readout

different technology, but same "large system" approach

Existing ICs are usually not directly applicable to ALS applications.

– however, 1st version of CAFE chip is being used in a high-rate photoelectron spectrometer (see C. Fadley's talk)

Immediate needs probably can be met by extensions of current systems using conventional technology.

Nevertheless, this is good time to review both goals and detector architectures.

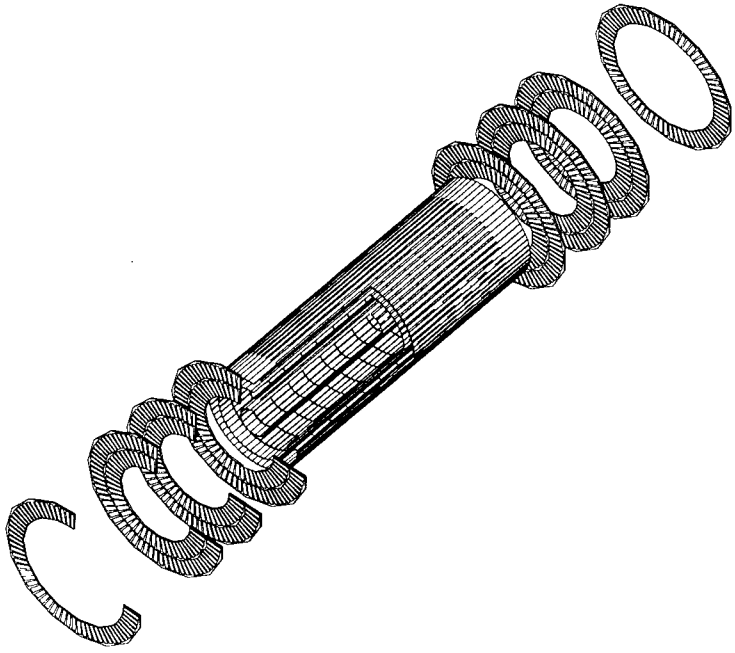
Are you exploiting the discovery potential of the machine?

Perhaps this will lead you in a direction that was precluded by the technical limits in the 60's and 70's, when the basic techniques were developed that are still in use today.

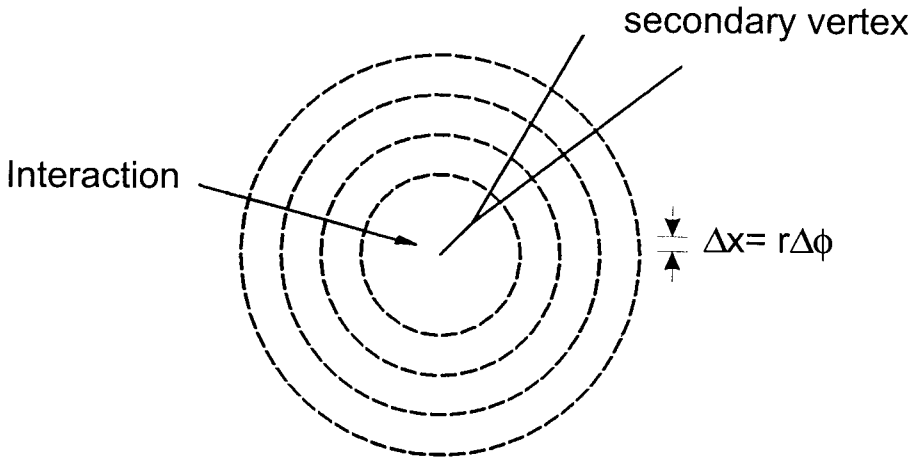
HEP Vertex Detectors

Full custom IC design for detectors was originally driven by the needs of vertex detectors in HEP

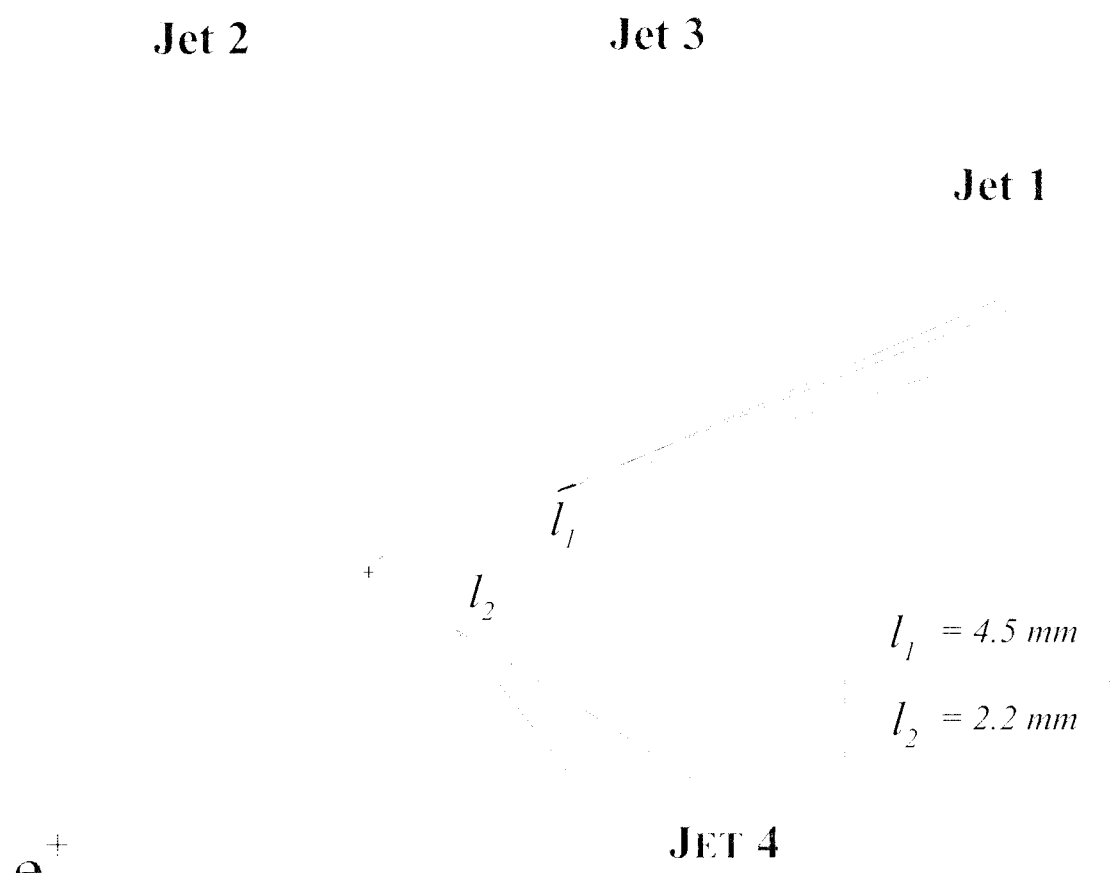
Typical configuration of a modern vertex detector



Resolution is provided primarily in azimuth, i.e.
radial electrodes in the disks,
electrodes parallel to the beam axis in the barrel:



$t\bar{t}$ Event
SVX DISPLAY
CDF



$M_{top}^{Fit} = 170 \pm 10$ GeV/c^2

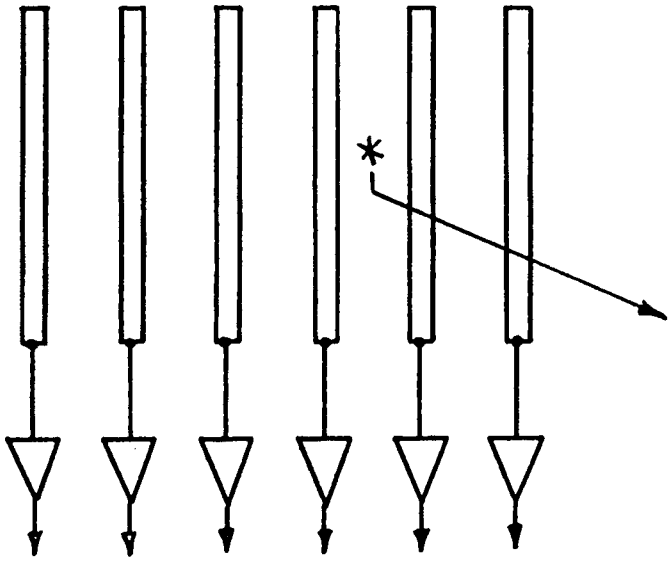
24 September, 1992
RUN #40758, EVENT #44414

Detectors with strip electrodes most commonly used

strip pitch: 25 – 100 μm

Two options:

Binary Readout



to discriminators

Position resolution determined directly by pitch

$$\sigma_x = pitch / \sqrt{12}$$

- optimize rate capability

Analog Readout

Interpolation yields resolution < pitch p

Relies on transverse diffusion

$$\sigma_x \propto \sqrt{t_{coll}}$$

e.g. in Si

$t_{coll} \approx$ 10 ns

$\Rightarrow$ $\sigma_x =$ 5 μm

Interpolation precision depends on S/N and p

$p =$ 25 μm and S/N=50

$\Rightarrow$ 3 – 4 μm resolution

- optimize resolution

Chips typically include

128 channels of

preamplifier
pulse shaping
pipeline to accommodate trigger latency
readout multiplexer

Channels laid out in parallel on ~50 μm pitch

IC ~ 6mm wide, typ. 4 – 8 mm long

Sparse data environment

many more detector elements than hits per event

⇒ on-chip sparsification (zero suppression)
(only struck channels are read out)

Critical Requirement: Minimize Material

⇒ low-mass shielding, cables, cooling

severe design challenge, as low-noise analog circuitry must operate simultaneously with digital circuitry on same chip.

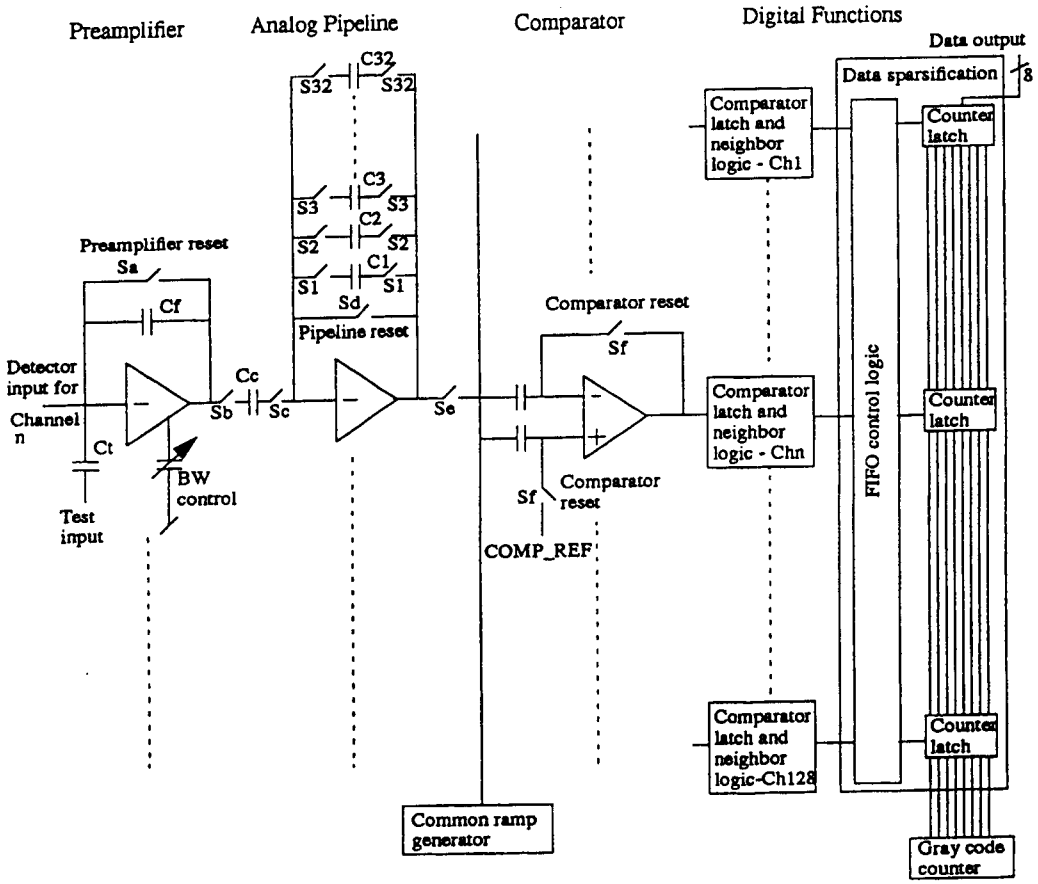
SVX2 and SVX3 (LBNL + FNAL)

Latest generation of readout chips for CDF and DØ at upgraded Tevatron (137 ns crossing time)

Include on-chip digitization of analog signal

Threshold, calibration via on-chip DACs

All communication to and from chip via digital bus



Wilkinson ADC integrated with pipeline + comparator required for sparsification. Adds 100 µm to length and 300 µW/ch power.

ADC clock runs at 106 MHz in experiment, tested to 400 MHz

Total power: 3 mW/ch

SVX2 die layout

Dimensions: 6.3 x 8.7 mm
0.8 μm, triple-metal rad-hard CMOS

Input Pads

Preamplifiers

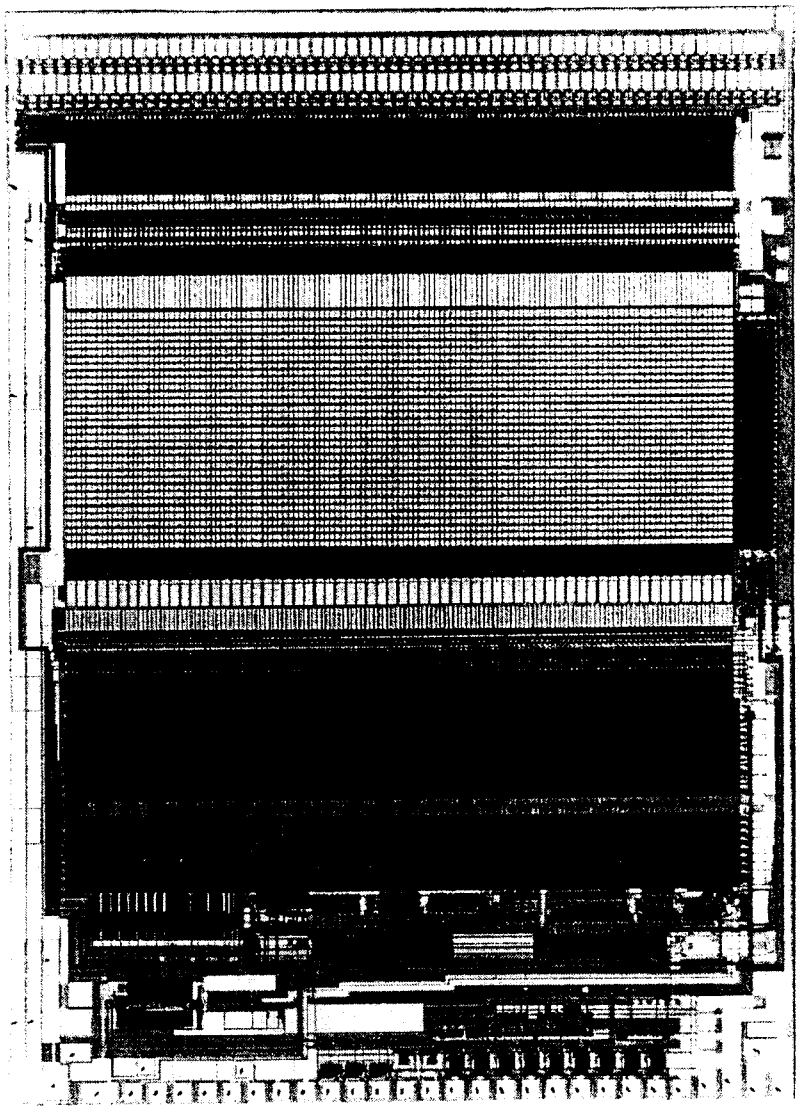
Analog Pipeline

ADC Comparator

Neighbor Logic

Sparsification + Readout

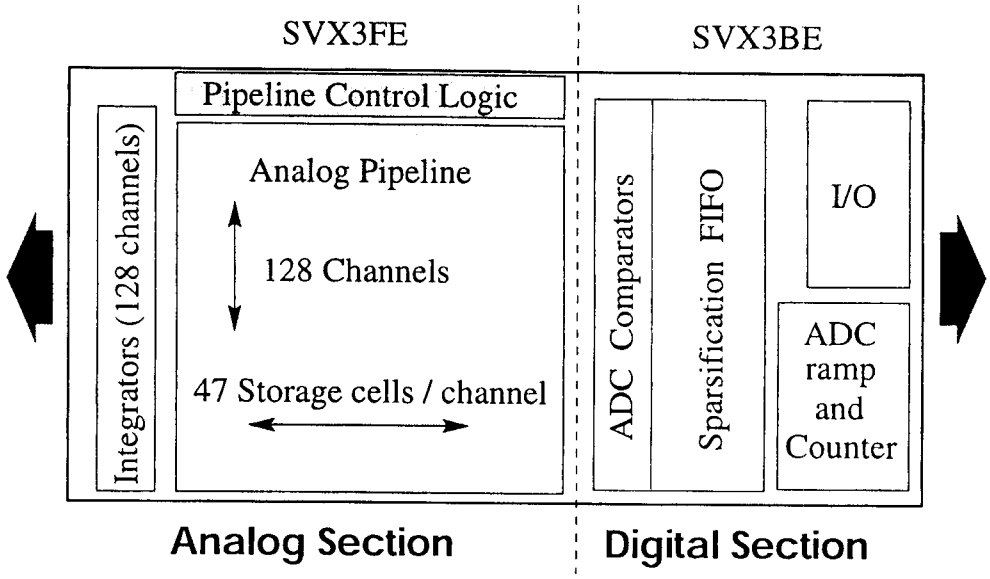
ADC Ramp + Counter, I/O



SVX2 (used by DØ) is designed for sequential signal acquisition and readout.

SVX3 (used by CDF) allows concurrent read-write, i.e. signal acquisition and readout can proceed concurrently.

SVX3 Floor Plan



Analog section: 6.26 x 8.06 mm^2
Digital section: 6.26 x 4.97 mm^2

Combined in 1 chip: 6.26 x 12 mm^2

Measured Noise: Q_n= 500 el + 60 el/pF rms

ATLAS Semiconductor Tracker (LHC)

Total rate of tracks in the detector: ~ $3 \cdot 10^{10}$ s^{-1}
(hit rate at $r_\perp$ = 14 cm: ~ 10^7 $cm^{-2}s^{-1}$)

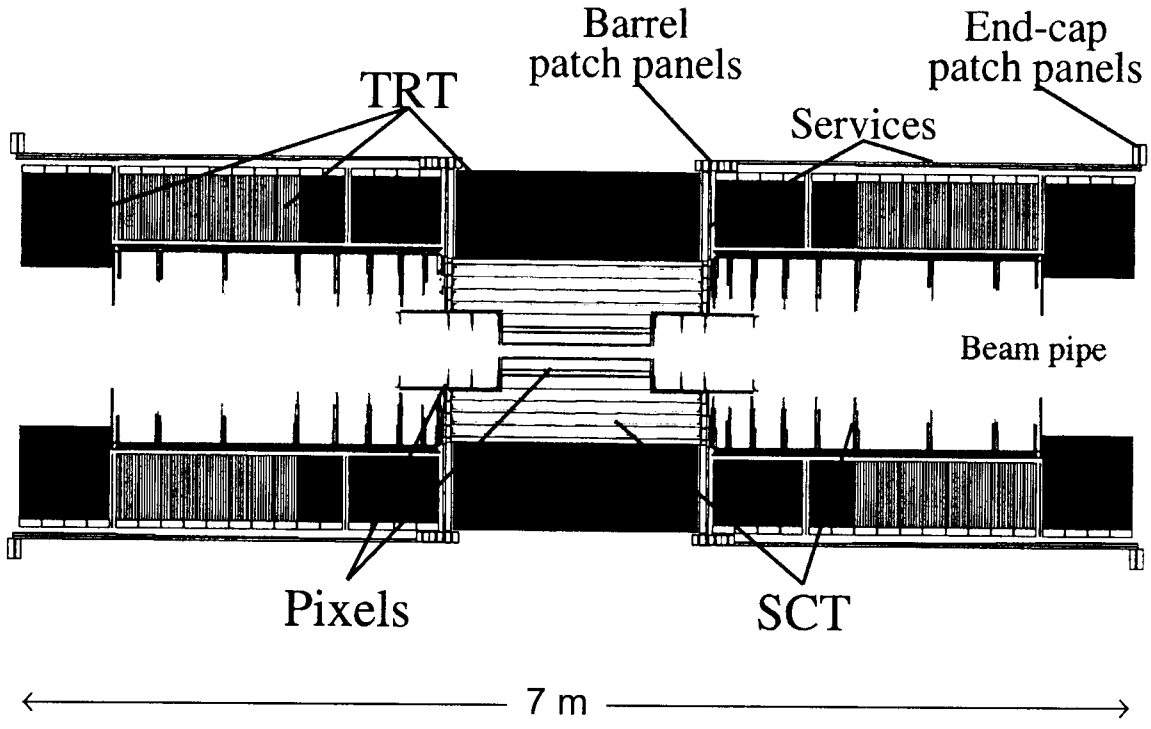
Pixels at small radii (4, 11, 14 cm) to cope with
- high event rate (2D non-projective structure)
- radiation damage

small capacitance ~ 100 fF $\Rightarrow$ low noise $Q_n \approx$ 200 el

Strips at larger radii (30, 37, 45, 52 cm) - minimize material, cost

Pixels and strips provide primary pattern recognition capability

Straw drift chambers at outer radius (56 – 107 cm)
~70 layers yield 40 space points at large r and augment pattern recognition by continuous tracking (least expensive solution)



Strip modules use back-to-back single-sided detectors with small-angle stereo (40 mr) to provide z-resolution with negligible "ghosting".

Resolution provided by 3 detector types in barrel

	$R\phi$	z
Pixels	12 μm	66 μm
Strips	16 μm	580 μm
Straws	170 μm	—

Segmentation ⇒ Large number of data channels

Total number of channels and area

Pixels	1.4×10^8 channels	2.3 m^2
Strips	6.2×10^6 channels	61 m^2
Straws	4.2×10^5 channels	

But, ...
only a small fraction of these channels are struck in a given crossing

Occupancy for pixels, 50 μm x 300 μm:

4 cm Pixel Layer	4.4×10^{-4}
11 cm Pixel Layer	0.6×10^{-4}

Occupancy for strip electrodes with 80 μm pitch, 12 cm length:

30 cm Strip Layer	6.1×10^{-3}
52 cm Strip Layer	3.4×10^{-3}

Strips + Pixels: many channels

Essential to minimize

power
material (chip size, power cables, readout lines)
cost (chip size)
failure rate (use simple, well controlled circuitry)

Goal is to obtain adequate position resolution, rather than the best possible

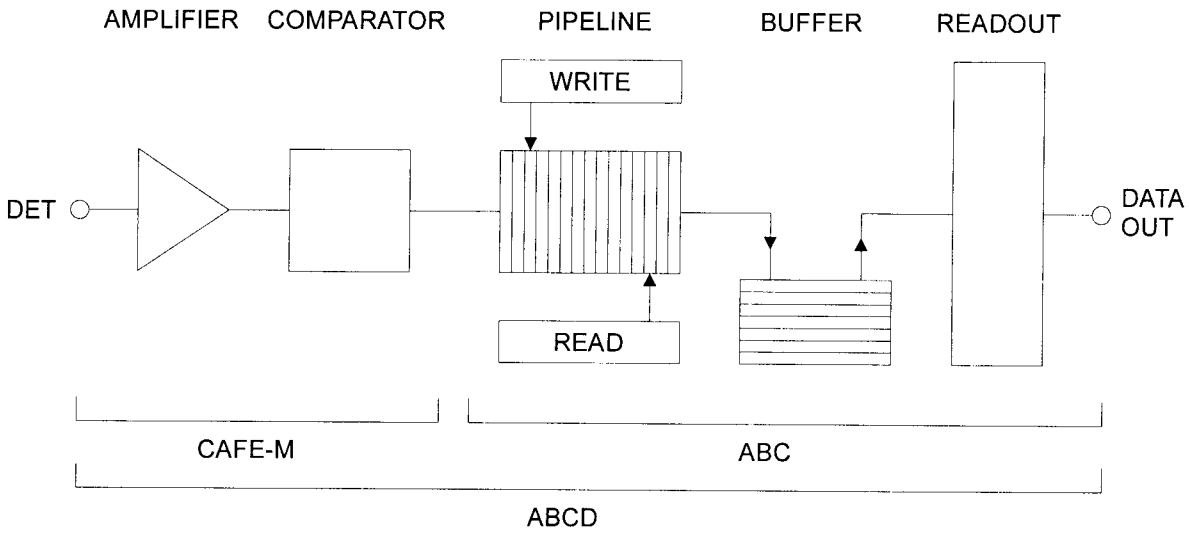
⇒ Binary Readout

detect only presence of hits

identify beam crossing

Architecture of ATLAS strip readout

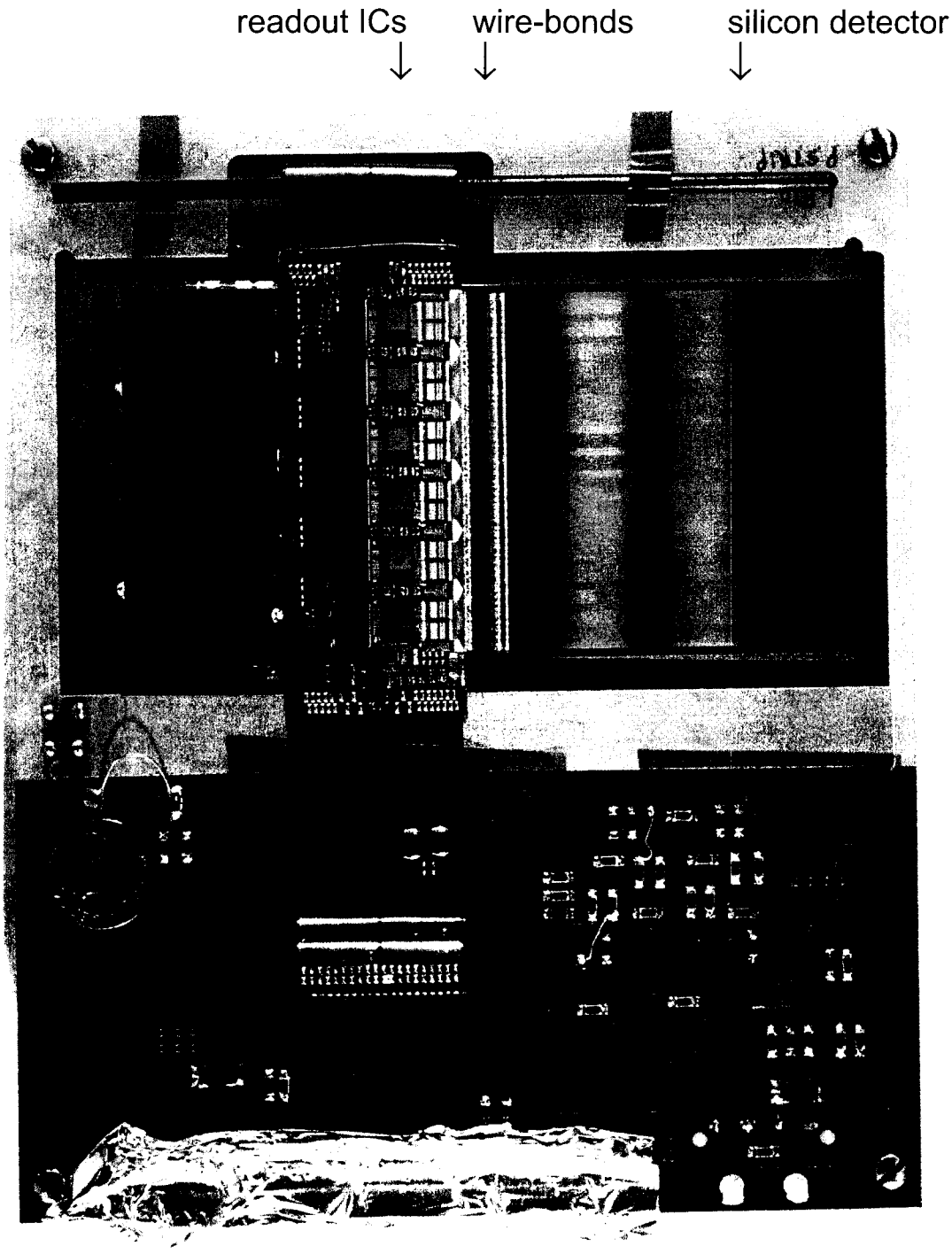
Pipeline clocked at LHC crossing frequency of 40 MHz



Two implementations with same functionality:

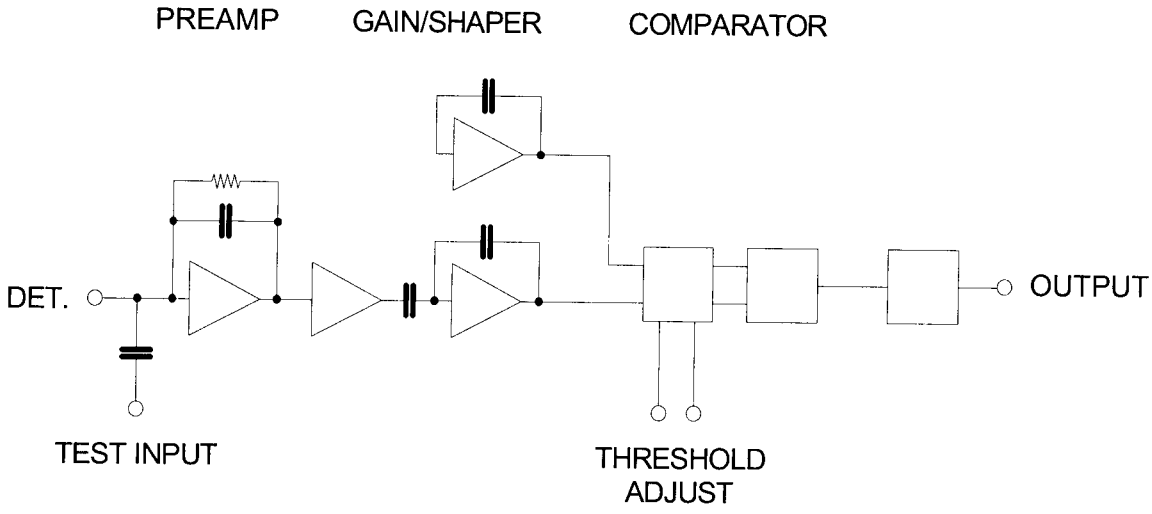
2 chips:	CAFE-M	(analog, BJT)	LBNL, UCSC
	+ ABC	(digital, CMOS)	RAL, UCSC, LBNL
1 chip:	ABCD	(analog + digital, BiCMOS)	Cracow, CERN, LBNL, RAL

ATLAS SCT test detector module



The module is mounted in a pc-board support frame to facilitate handling during test. The module itself is the rectangular object in the upper half of the picture.

Block diagram of CAFE chip
(LBNL, UCSC)



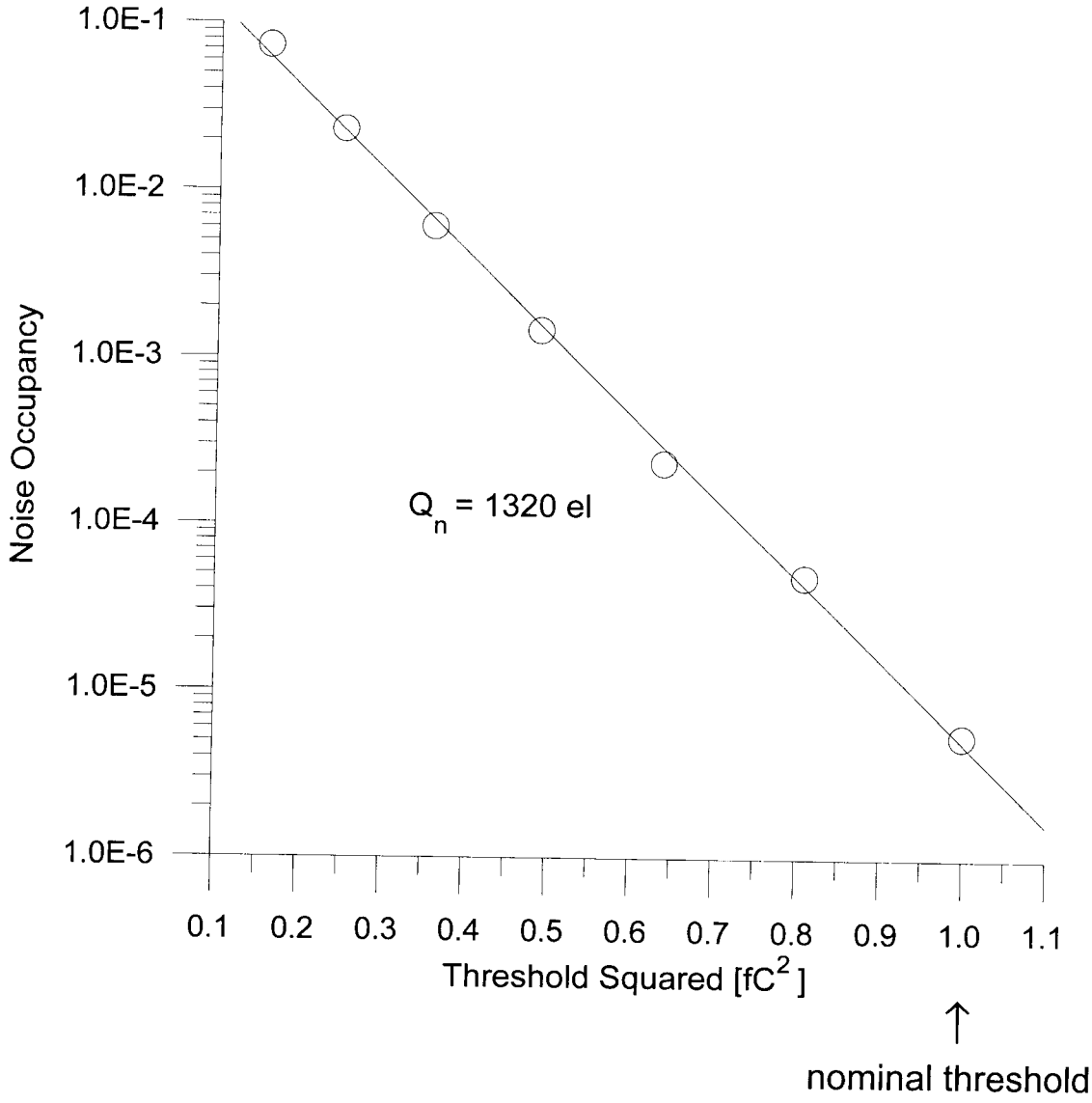
- 128 ch, bondable to 50 μm strip pitch
- bipolar transistor technology, rad-hard
  ⇒ minimum noise independent of shaping time*
- peaking time: 25 ns (equivalent CR-RC^4)
- double-pulse resolution (4 fC – 4 fC): 50 ns
- 1300 el rms noise, <25 ns timing (>99% of hits)
- 1.3 to 1.8 mW/ch (current in input transistor adjustable)
- die size: 6.4 x 4.5 mm^2

see: I. Kipnis, H. Spieler and T. Collins, IEEE Trans. Nucl. Sci. **NS-41/4** (1994) 1095-1103
and http://www-atlas.lbl.gov/strips/strips.html for more info.

* see http://www-physics.lbl.gov/~spieler/physics_198_notes.html

Noise Occupancy vs. Threshold

Module with CAFE chip in test beam position at KEK



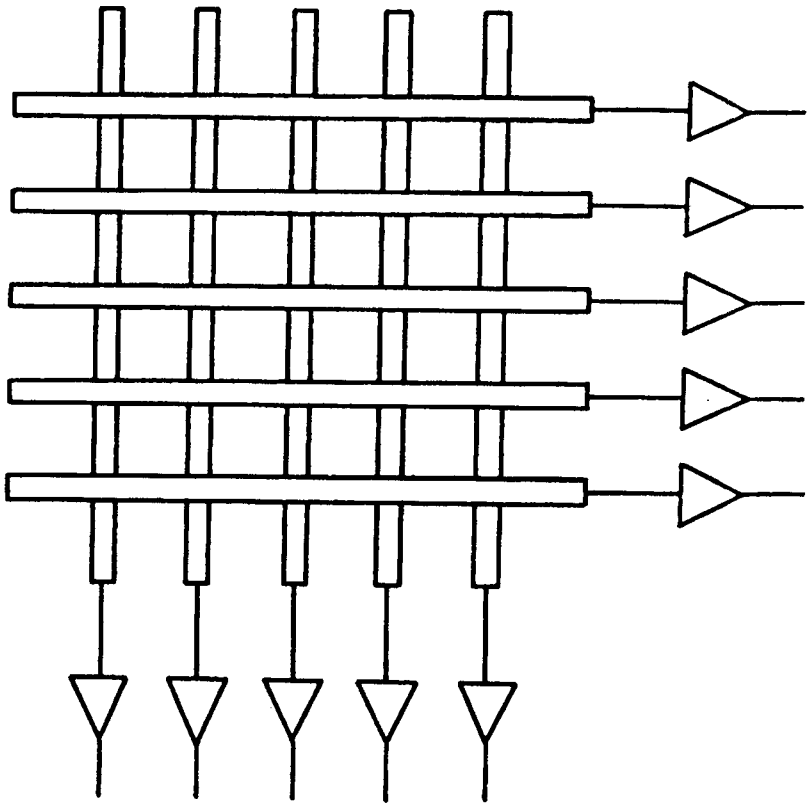
non-random baseline fluctuations, digital cross-talk

⇒ deviations from straight line plot (gaussian noise)

Measured performance of modules in test beams within few % of theoretical predictions.

Two-Dimensional Detector

Example: Crossed strips on opposite sides of Si wafer



n readout channels $\Rightarrow$ n^2 resolution elements

Problem: ambiguities with multiple hits

n hits in acceptance field $\Rightarrow$ n x-coordinates
n y-coordinates

$\Rightarrow$ n^2 combinations

of which
$n^2 - n$ are "ghosts"

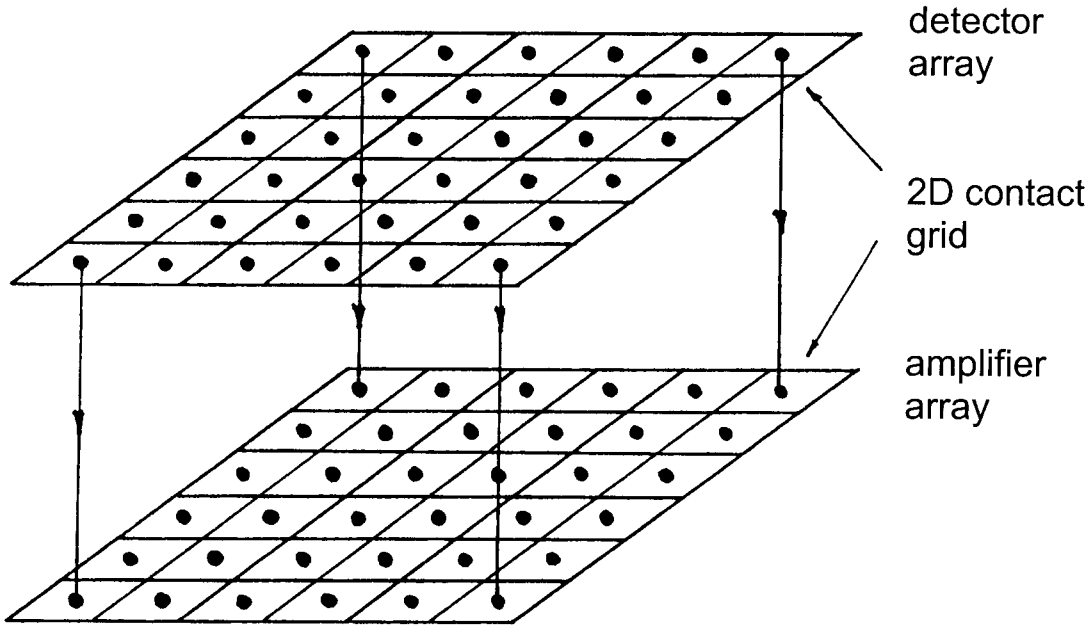
ATLAS reduces ambiguities by using small angle stereo (40 mrad).

Not sufficient at small radii – need non-projective 2D detector

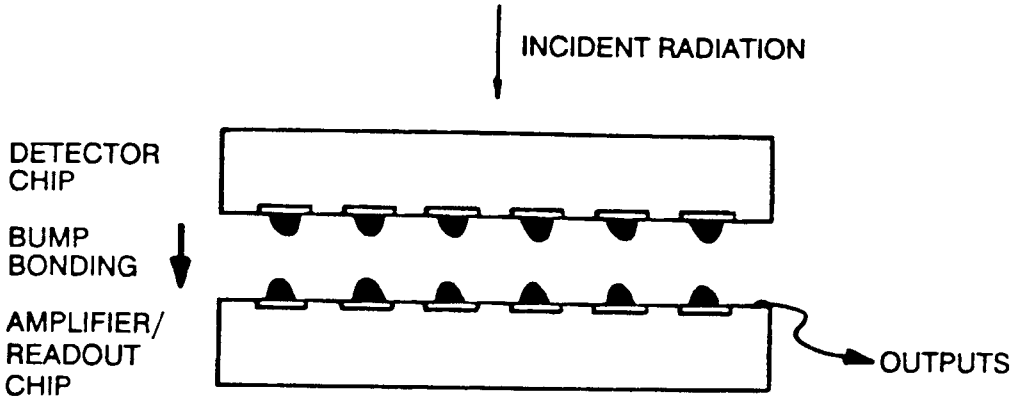
Pixel Detectors with Random Access Readout

Amplifier per pixel

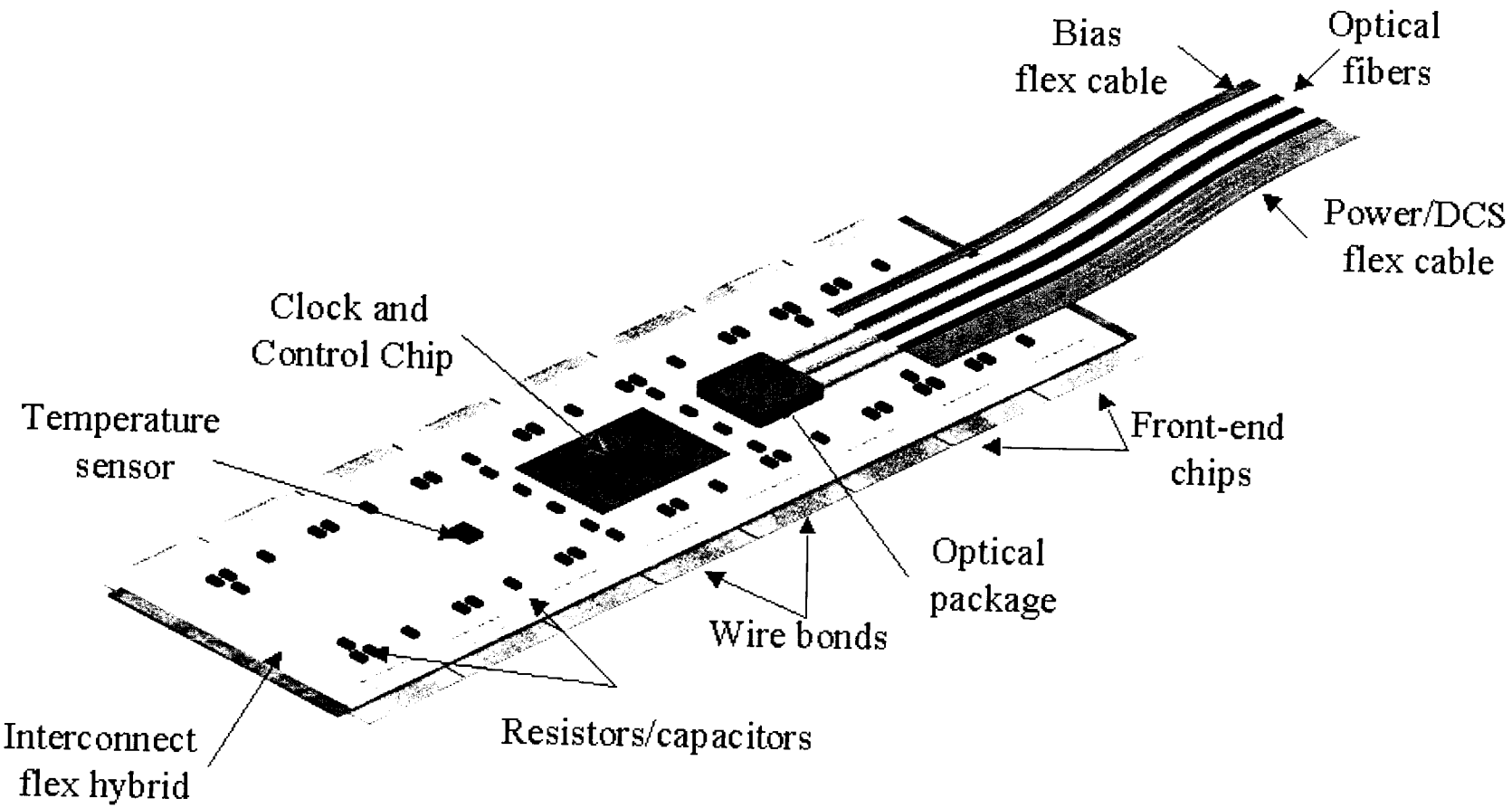
Address + signal lines read out individually addressed, i.e. single, pixels



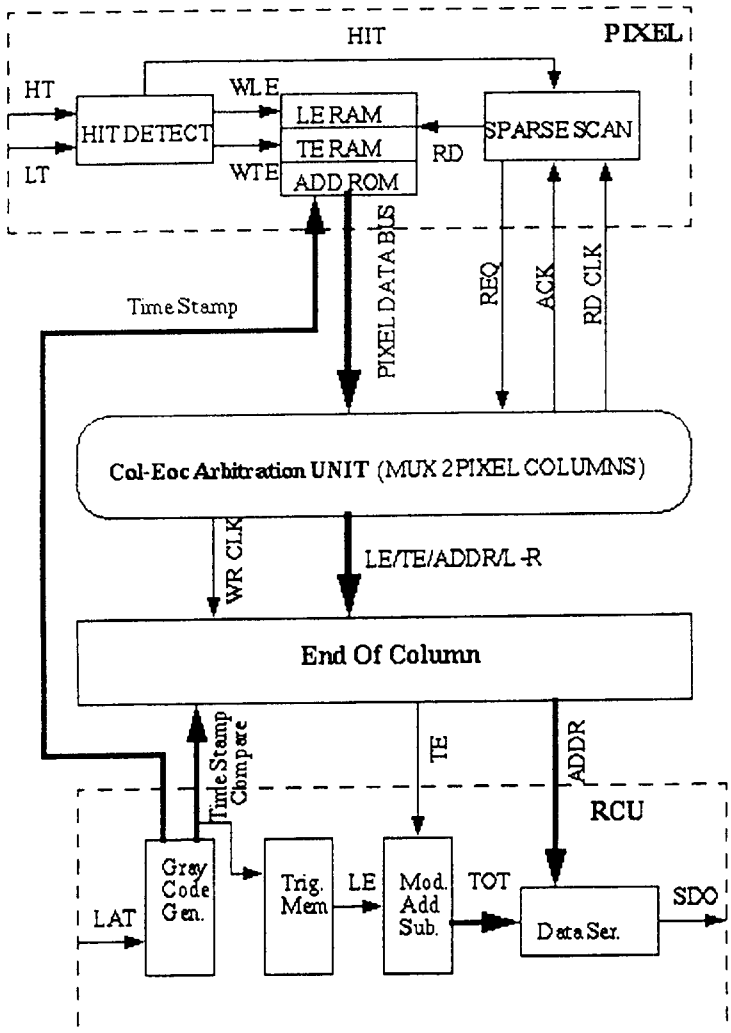
2D contact via "bump bonds"



"Mature technology", but ATLAS had to go through a painful multi-year process before finding a set of reliable vendors.


Bias
flex cable
Optical
fibers
Power/DCS
flex cable
Clock and
Control Chip
Temperature
sensor
Front-end
chips
Optical
package
Wire bonds
Interconnect
flex hybrid
Resistors/capacitors

Fast Pixel Readout for ATLAS (LBNL, K. Einsweiler, et al.)

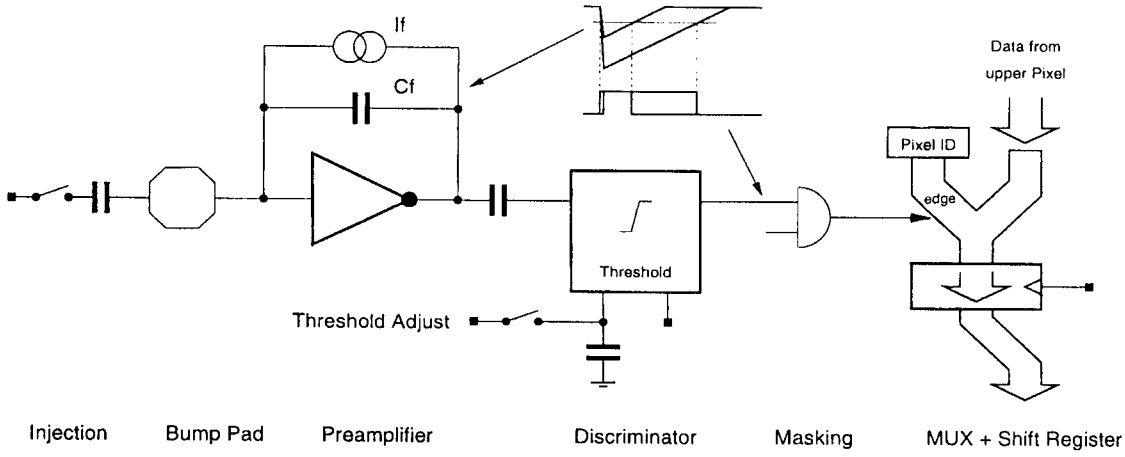


Quiescent state: no clocks or switching in pixel array

When pixel is struck: pixel address is sent to column buffer at chip periphery and time stamped

Receipt of trigger: check to see which addresses are in selected time bin and selectively read out pixels.

Block Diagram of Pixel Cell



Linear discharge of preamplifier feedback capacitor provides linear time-over-threshold digitization for readout of analog information.

Pixel size: 50 μm x 300 μm

Power per pixel: < 40 μW

Final chip: 24 columns x 160 pixels (3840 pixels)

Module size: 16.4 x 60.4 mm^2

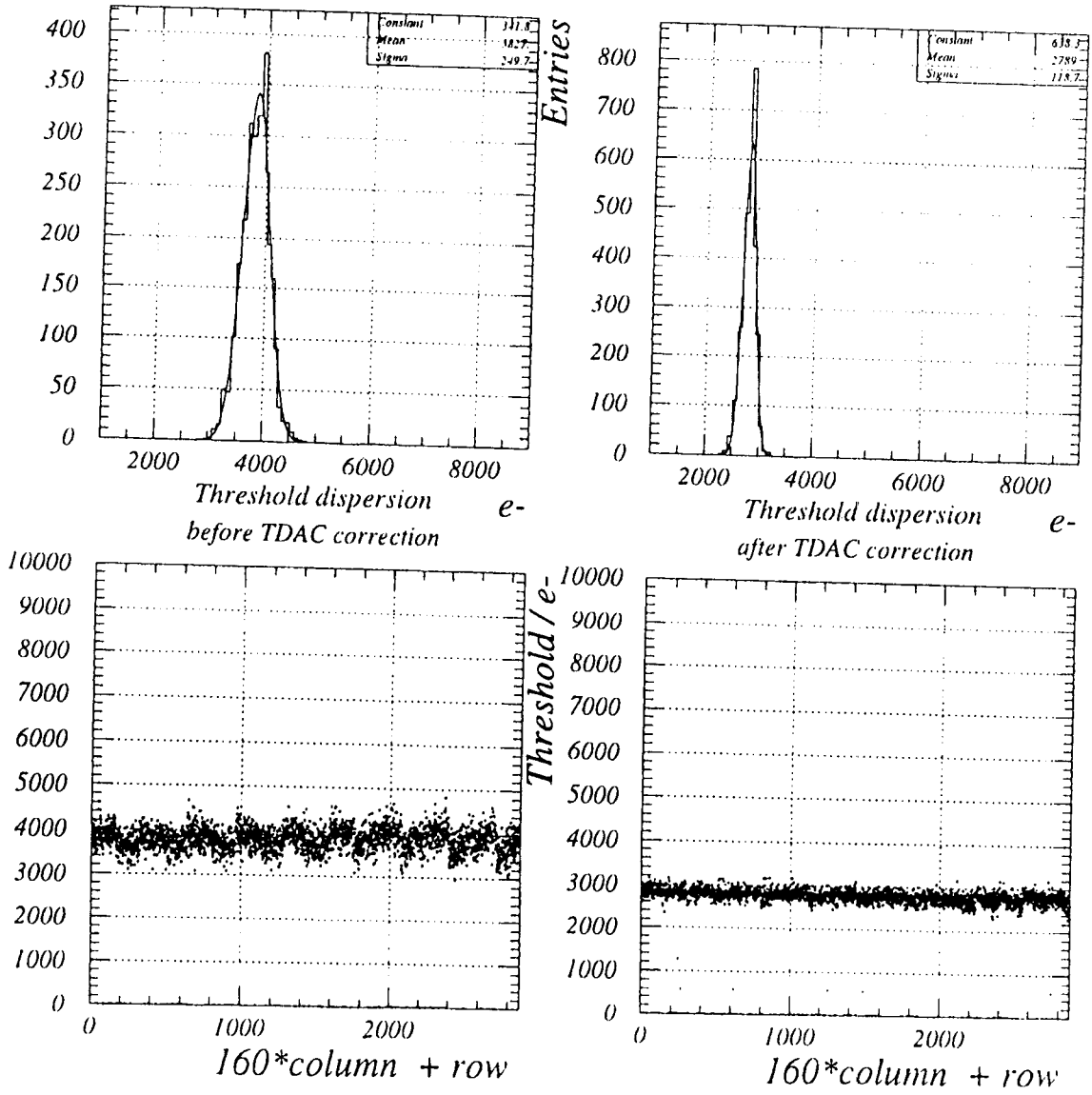
16 front-end chips per module

61440 pixels per module

Pixel size required because of radiation hardness and event rate requirements.

Low power + space constraints ⇒ excessive pixel-to-pixel threshold variations

All thresholds can be trimmed continually pixel by pixel to maintain uniformity in the course of radiation damage (software, automated).



I have seen the future, and it works.

Lincoln Steffens

This was written in St. Petersburg, Russia during the October Revolution

⇒ It takes more than a grand vision

II. Some Common Problems

a) The Design and Debugging Process

Example: CAFE Chip for ATLAS Experiment at LHC (CERN)

Participants (people who really did the work):

Alessandra Ciocio	LBNL	Staff Scientist
John Emes	LBNL	Technician
Carl Haber	LBNL	Sr. Physicist
Issy Kipnis	LBNL	Sr. Elec. Engineer
Jim Siegrist	LBNL	Sr. Faculty Physicist
Marjorie Shapiro	LBNL	Sr. Faculty Physicist
Ned Spencer	UCSC	Elec. Engineer
Helmuth Spieler	LBNL	Sr. Physicist

within larger collaboration

Major Tasks

1. Define requirements and design circuit (Kipnis, Spencer, Spieler)

   This is an interactive process!

   You can't just define requirements without considering the architecture and the technology.

   Design Reviews crucial.

   Concurrently: design hybrid to ensure proper placement of bond pads (Haber)

2. Chip is fabricated by foundry (AT&T)

   ICs delivered untested on undiced wafers

3. Wafer testing (Emes, Shapiro, Siegrist, Spieler)

   test all critical parameters on all 128 channels per chip
   about 250 chips per wafer
   uses specially designed electronics + DAQ

   often uncovers process problems – interact with wafer fab

4. Assemble and test data acquisition system (Ciocio)
   DAQ system designed at UCSC + UCI

5. Assemble hybrid (Emes, Haber)

6. Test hybrid (Ciocio, Haber, Spieler)

7. Mount hybrid on detector
   (detectors fabricated in LBNL Micro-Systems Lab)

8. Test module … debug … test module … (Ciocio, Haber, Spieler)

9. Beam Tests at CERN, KEK
   (Ciocio, Haber, Shapiro, Siegrist, Spieler)

   Typically test several modules with several thousand channels

   Verify performance in experimental environment

   Collaborative effort with groups from other labs, countries, continents

10. Scrutinize data, find circuit improvements, redesign based on new spec's.

    … back to 1.

This was for a set of prototype chips designed as iterations towards the final design.

Similar process now underway for final chip adopted by collaboration.

Lessons Learned

personal observationsfrom my own work + from experience as project reviewer/advisor for numerous HEP detectors in US, Europe, Japan

1. Total required effort is always underestimated

vicious circle: project budgets are "low-balled" to get accepted by scientific management (even when not clueless in technical matters)

$\Rightarrow$ inadequate resources for good design

$\Rightarrow$ marginal design incurs avoidable problems, rework, redesign

$\Rightarrow$ project costs more than it would have, if properly set up from the start

2. Inadequate engineering resources

3. Chips may be "functional", but unusable

testing and debugging not considered during design

4. Good documentation requires effort – usually inadequate

5. Biggest technical problem is electro-mechanical integration

Examples: hybrids (severely underappreciated)
mounting + cooling
cabling

These components require expertise in both electronics and mechanics – engineers aren't educated that way.

Usually done by physicists.

What does it take?

1. Realization that these are complex systems

   Although a detector module is only cm^2 in size, its development can require 10s of FTEs

2. The appropriate architecture and technology

   the newest technology is not necessarily the best

   experiments must balance wishes vs. technical effort

   avoid the "wouldn't it be nice" syndrome

   match sophistication of technology to experience

   use "debuggable technology"

   example: wire bonds can be pulled and redone
   bump bonds are unforgiving

   short turn-around times for prototypes

   $\Rightarrow$ gain experience with "simple" systems,

   then step up to greater complexity

   (e.g. first 1D, then 2D systems)

3. A strong interdisciplinary team, consisting of

   scientifically astute engineers + technically astute scientists

   All successful HEP detectors are a team effort between engineers, technicians and scientists.

   It is crucial that scientists dig into technical details.

What does it take? cont'd

4. Adequate funding + the right people

contrary to common lore, finding the right people is more difficult than finding the funding.

Note: "adequate resources" does not necessarily mean "huge resources"

Large HEP collaborations consist of many small groups, but they work together and share knowledge + resources.

Physics Division has concurrently worked on major Si detectors for BaBar, CDF, DØ and ATLAS, all of which are different.

Separate groups, but experience and equipment were shared.

5. The willingness to work with other groups

HEP has strong tradition of information exchange.

Major developments (e.g. pixel detectors) only possible by leveraging from work of other groups.

Sociology

1. the resource myth

   good work can be done with modest funding

   the key ingredient in IC detector development is not money, but the ability to use money effectively.

   most important is

   - intellectual capital

   Requires

   - willingness to learn (anything and everything)
   - good circuit designers
   - good systems engineers/physicists
   - physicists who understand the technology and can communicate with engineers

2. the big group myth

   - most chips developed in small groups
   - many good IC developments by university groups

   exception: "complex" chips (e.g. pixel readout)

3. evolution and synergy

   circuits as building blocks (don't reinvent everything)
   cross-fertilization between fields

   - new applications can adapt existing techniques

   Examples: both PET and x-ray chips used HEP circuits tailored to specific requirements

   Novel CCDs for astronomy developed at LBNL Microsystems Lab are a spin-off from SSC detector R&D

4. instrumentation as commodity

- vanishing expertise
- instrumentation development tends to be funded as part of construction projects

⇒ discourages risk-taking and innovation (deadlines, budgets predicated on production)

⇒ Research groups and funding agencies must support detector development as research area

5. Labs/Divisions must sustain technical base independently of specific programs

Physics Division has supported Micro-Systems Lab as an R&D facility and general scientific resource, *without receiving additional funding from DOE.*

Payoff: SNAP

major scientific project that will revolutionize field

result of many "small" developments, not of grandiose "master plan"

6. discovery potential

conventional thinking leads to conventional experiments